LOW JITTER CLOCK FOR A PHYSICAL MEDIA ACCESS SUBLAYER ON A FIELD PROGRAMMABLE GATE ARRAY

ABSTRACT

A programmable logic device (PLD) is provided that supports multi-gigabit transceivers (MGTs). The PLD includes one or more pairs of shared clock pads for receiving one or more high-quality differential clock signals. Dedicated clock traces couple each pair of shared clock pads to one or more MGTs on the PLD. Each MGT includes a clock multiplexer circuit, which allows one of the high-quality differential clock signals to be routed as a reference clock signal for the MGT. The clock multiplexer circuits are designed such that no significant jitter is added to the high-quality clock signals. The clock multiplexer circuits can also route general-purpose clock signals received by the PLD as lower quality reference clock signals for the MGTs. The reference clock signal routed by the clock multiplexer circuit can be stepped down to provide a reference clock for a physical coding sublayer of the MGT.